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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,930	08/29/2003	Jun Koyama	12732-164001	7988
26171	7590	09/15/2006	EXAMINER	
FISH & RICHARDSON P.C. P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			NGUYEN, KIMNHUNG T	
			ART UNIT	PAPER NUMBER
			2629	

DATE MAILED: 09/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/650,930	Applicant(s) KOYAMA ET AL.	
	Examiner Kimnhung Nguyen	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 September 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-60 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5,6,11,12,17,18,23,24,29,30,35,36,41,42,47,48,53,54,59 and 60 is/are allowed.
- 6) ☒ Claim(s) 1-4,7-10,13-16,19-22,25-28,31-34,37-40,43-46,49-52 and 55-58 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>9/5/06</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114.

Applicant's submission filed on 9/5/06 has been entered.

2. The indicated allowability of claims 1-4, 7-10, 13-16, 19-22, 25-28 and 31-34, 37-40, 43-46, 49-52 and 55-58 are withdrawn in view of the newly discovered reference(s) to Sasaki (US 6,049,321). Rejections based on the newly cited reference(s) follow.
3. This application has been examined. The claims 1-60 are pending. The examination results are as following.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 7-8, 13-14, 25, 26, 31, 32, 37, 38, 43, 44, 49, 50, 55, 56 are rejected under 35 U.S.C. 102(b) as being anticipated by Sasaki (US 6,049,321 admitted by applicant).

As to claims 1-2 and 25-26, Sasaki discloses in fig. 1, a liquid crystal display device having on an insulating substrate a plurality of source signal lines (S1, S2), a plurality of gate

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signal lines (X1-X4), a plurality of pixels, and a source signal line driver circuit for driving the source signal lines, wherein the source signal line driver circuit has a plurality of analog buffer circuits (35, 36), wherein a switching circuit (37) is provided between the analog buffer circuits and the source signal lines (S1, S2), wherein the plurality of source signal lines (S1, S2) and the plurality of analog buffer (35, 36) circuit constitute a circuit group, and wherein a connection between one of the source signal lines (S1) and one (35) of the analog buffer circuits (35, 35) is periodically switched to a connection between the one of the source signal lines and another one (36) of the analog buffer circuits (35, 36) by any one of the switches.

Regarding claims 7-8, 13-14, 31, 32, 37, 38; Sasaki discloses further wherein the analog buffer circuits are source follower circuits.

Regarding claim 43-44, Sasaki discloses further in fig. 2, wherein the switching circuit comprises an analog switching circuit (see analog buffer switch 214, see fig. 2).

Regarding claims 49, 50, 55, 56, Sasaki discloses further, wherein a first source signal line (S1) is connected to a first analog buffer circuit (35) via a first connection point of one of the switches in a first period, and the first source signal line is connected to a second analog buffer circuit (36) via a second connection point of the other one of the switches in a second period.

Regarding claims 19, 20, Sasaki discloses further, electronic equipment comprising a liquid crystal display device (see fig. 1).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

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having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 3-4, 9, 10, 15, 16, 27-28, 33, 34, 39, 40 and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki (US 6,049,321) in view of Youn (US 2002/0089485).

Regarding claims 3-4, 27-28, Sasaki does not disclose a set of n periods is periodically repeated in a random timing.

Youn discloses in figs. 3-4, a set of n periods is periodically repeated in a random timing (see a source signal line (drive data) having an inversion drive repeating in a period of two frames, see 0061).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement a set of n periods is periodically repeated as taught by Youn into the system of Sasaki because this would shift down every one line as frame changes and thus to eliminate flickering that may take place in the dot pattern of the device system (see 0061-0062).

Regarding claims 9, 10, 15, 16, 33, 34, 39, 40, Sasaki discloses further in fig. 1, wherein the analog buffer circuit (35, 36) are source follower circuits.

Regarding claims 45-46, Sasaki discloses further in fig. 1, wherein the switching circuit comprises an analog switching circuit (see 35, 36, see fig. 1).

Regarding claims 51, 52, 57, 58, Sasaki discloses further, wherein a first source signal line (S1) is connected to a first analog buffer circuit (35) via a first connection point of one of the switches in a first period, and the first source signal line is connected to a second analog buffer circuit (36) via a second connection point of the other one of the switches in a second period.

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Regarding claims 21, 22, Sasaki discloses further, electronic equipment comprising a liquid crystal display device (see fig. 1).

Allowable Subject Matter

8. Claims 5-6, 11-12, 17-18, 23-24, 29-30, 35-36, 41-42, 47-48, 53-54 and 59-60 are allowed.


9. The following is an examiner's statement of reasons for allowance: The present invention is directed to a liquid crystal display having on an insulating substrate a plurality of source signal lines, a plurality of gate signal lines, a plurality of pixels, and a source signal line driver circuit for driving the source signal lines, wherein the source signal line driver circuit has a plurality of analog buffer circuits, wherein a switching circuit having switches is provided between the analog buffer circuits and the source signal lines, wherein the plurality of source signal lines and the plurality of analog buffer circuits constitute a circuit group. The closest prior art of Chiang ((2002/0063674) shows a similar invention, however, he fails to teach that wherein a switching circuit is provided between the analog buffer circuits and the source signal lines, wherein n (n is a natural number and is equal to or larger than 2) source signal lines and n analog buffer circuits constitute a circuit group, wherein a set of n periods is periodically repeated, and wherein, in an r-th period, the switching circuit connects an m-th source signal line in the circuit group to an (m+r-1)-th analog buffer circuit and an l-th source signal line to an (1-n+r-1)-th analog buffer circuit, respectively as claims 5-6, 29-30.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimnhung Nguyen whose telephone number is (571) 272-7698. The examiner can normally be reached on MON-FRI, FROM 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Kimnhung Nguyen
Patent Examiner
September 12, 2006